What is Claimed is:

1. An I/O compression test circuit for compression testing data loaded on a plurality of global I/O lines, comprising:

a plurality of test blocks for testing a plurality of global I/O line groups depending on a test enable signal, wherein the plurality of global I/O lines are divided into the plurality of global I/O line groups;

a decision block for deciding a test result in response to output signals from the plurality of test blocks;

a driving block for outputting a test result signal in response to a decision signal outputted from the decision block; and

a control block for controlling a test timing of the test blocks, initializing an input terminal of the decision block and controlling a driving timing of the driving block.

2. The circuit according to claim 1, wherein the test block comprises:

a logic means for performing a logic operation on a compression test enable signal, a test block enable signal and a test timing control signal;

a first test means for outputting a first level when at least one of data transmitted into the global I/O line group is at a different level depending on an output signal from the logic means; and

a second test means for outputting a second level when at least one of data transmitted into the global I/O line group is at a different level depending on an output signal from the logic means.

3. The circuit according to claim 2, wherein the decision block comprises:

a first input terminal connected in common to an output terminal of the first test means of the test block;

a second input terminal connected in common to an output terminal of the second test means of the test block;

a first transmission means for selectively transmitting a potential of the first input terminal depending on a potential of the second input terminal; and

a second transmission means for selectively transmitting a signal having an inverted potential of the first input terminal depending on a potential of the second input terminal.

4. The circuit according to claim 3, wherein the

decision block further comprises:

a first latch means for maintaining a potential of the first input terminal; and

a second latch means for maintaining a potential of the second input terminal.

5. The circuit according to claim 3, wherein the decision block further comprises:

a first initialization means for selectively initializing a potential of the first input terminal to the first level depending on an reset signal outputted from the control block; and

a second initialization means for selectively initializing a potential of the second input terminal to the second level depending on the reset signal.

6. The circuit according to claim 1, wherein the driving block comprises:

a transmission means for selectively transmitting an driving control signal outputted from the decision block synchronously with respect to an output signal from the control block; and

a driving means for pulling up or down an output terminal in response to a signal selectively transmitted by

the transmission means.

7. The circuit according to claim 6, wherein the driving block further comprises a latch means for maintaining a potential of the output terminal.

8. The circuit according to claim 1, wherein the control block comprises:

a strobe signal generator for generating a strobe signal in response to a compression test enable signal and a detecting signal, wherein the strobe signal controls a test timing of the test timing, wherein the detecting signal is activated when data are loaded on the global I/O line;

an initialization signal generator for generating an initialization signal in response to the compression test enable signal and the detecting signal, wherein the initialization signal initializes an input terminal of the decision block to a predetermined level; and

a driving control signal generator for generating a driving control signal in response to the strobe signal.

9. The circuit according to claim 8, wherein the strobe signal generator comprises:

a logic means for performing a logic operation on the compression test enable signal and the detecting signal; and

a pulse generator for outputting a pulse signal in response to an output signal from the logic means.

10. The circuit according to claim 8, wherein the initialization signal generator comprises:

a first logic means for performing a logic operation on the compression test enable signal and the detecting signal; and

a second logic means for performing a logic operation on the compression test enable signal and an output signal from the first logic means.

11. The circuit according to claim 8, wherein the driving control signal generator comprises a delay means for delaying the strobe signal.